

## Course Description

Learn to increase design performance and achieve repeatable results by using the PlanAhead™ software tool. Topics include: a product overview, synthesis and project tips, design analysis, creating a floorplan, improving performance, experimenting with implementation options, incremental methodology, block-based IP design, and I/O pin assignment.

**Note:** The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and demos.

**Level** – FPGA 3

**Course Duration** – 2 days

**Price** –

**Course Part Number** – FPGA11000-11-ILT

**Who Should Attend?** – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

**Prerequisites**

- *Fundamentals of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Designing for Performance* recommended

**Software Tools**

- Xilinx ISE® Design Suite: Logic or System Edition 11.1

After completing this comprehensive training, you will have the necessary skills to:

- List the main features and benefits of the PlanAhead tool
- Import designs into the PlanAhead tool project environment
- Assign optimal I/O pin locations
- Import HDL sources and elaborate and analyze an RTL netlist
- Analyze design statistics, connectivity, timing, and placement results
- Run the Design Rule Checker (DRC) and Weighted Average Simultaneous Switching Output (WASSO) analysis
- Partition and floorplan designs
- Run ExploreAhead to try multiple implementation strategies
- Import and analyze the implementation results to improve the floorplan
- Floorplan to improve performance and consistency
- Use block-based design and create reusable IP

## Course Outline

### Day 1

- Course Overview
- **Lab 1:** Getting Started with the PlanAhead Tool
- I/O Pin Planning
- **Lab 2:** Assigning I/O Pins
- Design Analysis and Exploration
- **Lab 3:** Design Analysis and Exploration
- Design Partitioning and Top-Level Floorplanning
- **Lab 4:** Design Partitioning and Top-Level Floorplanning

### Day 2

- Implementing a Floorplanned Design
- **Lab 5:** Implementation
- Floorplanning Techniques
- **Lab 6:** Floorplanning

- Tuning a Floorplan for Performance
- **Lab 7:** Floorplan Tuning
- Block-Based Design and IP Reuse
- **Lab 8:** Block-Based Design and IP Reuse
- Floorplanning Strategies
- Course Summary

## Lab Descriptions

**Note:** All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.

- **Lab 1:** Getting Started with the PlanAhead Tool – Illustrates the steps you take to import a synthesized design into the PlanAhead tool so that you can begin floorplanning. Also introduces the PlanAhead tool environment and views.
- **Lab 2:** Assigning I/O Pins – Introduces the PinAhead environment for performing I/O pin assignment. You will create a project, import and export I/O ports lists, create I/O ports and interfaces, and make pin assignments.
- **Lab 3:** Design Analysis and Exploration – Introduces the analysis features of the PlanAhead tool that enable early detection of potential design issues, alternate device selection, initial floorplanning direction, and post-implementation exploration.
- **Lab 4:** Design Partitioning – Introduces the concept of floorplanning. By using automated partitioning tools, you will create a top-level floorplan and experiment with sizing and shaping Pblocks based on resources assigned to them.
- **Lab 5:** Implementation – Introduces the integration of the ISE software implementation tools with the PlanAhead tool. Also introduces the ExploreAhead tool for queuing multiple ISE software runs with varying strategies.
- **Lab 6:** Floorplanning – Describes how to analyze implementation results and to use that information to generate a floorplan aimed at increasing design performance.
- **Lab 7:** Floorplan Tuning – Introduces techniques to help close on timing targets consistently.
- **Lab 8:** Block-Based Design and IP Reuse – Describes the steps to implement a block-based methodology that includes the creation and reuse of an IP module.

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